IN THE CLAIMS:

Claim 18 has been amended herein to include the change from the Examiner's Amendment, which contained a typographical error in that it amended Claim 8 instead of Claim 18. All of the pending claims 1 through 22 are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

1. (Previously presented) A method for assembling a multidie semiconductor device package, comprising:

providing an interposer with a substantially planar substrate and a receptacle formed substantially through the substrate, the substrate having an upper surface and a lower surface, at least the upper surface having conductors thereon;

positioning at least one first-level semiconductor device within the receptacle, a backside of the at least one first-level semiconductor device being substantially coplanar with the lower surface of the substrate or located within a plane which extends through the substrate an interstitial space remaining at least between peripheral edges of the at least one first-level semiconductor device and the substrate;

positioning a second-level semiconductor device above the upper surface of the substrate, a portion of the second-level semiconductor device superimposed with the upper surface of the substrate;

electrically connecting the at least one first-level semiconductor device to at least the conductors on the upper surface of the substrate by first-level conductive members that include laterally extending portions that are at least partially carried by a surface of the second-level semiconductor device; and

electrically connecting the second-level semiconductor device to the conductors on the upper surface of the substrate by second-level conductive members.

2. (Original) The method of claim 1, further comprising introducing a quantity of encapsulant material into the receptacle so as to fill at least a portion of the interstitial space.

3. (Previously presented) The method of claim 2, wherein the introducing encapsulant material is effected after the electrically connecting the at least one first-level semiconductor device.

4. (Original) The method of claim 2, further comprising introducing a quantity of encapsulant material between the second-level semiconductor device and the at least one first-level semiconductor device.

5. (Previously presented) The method of claim 1, wherein electrically connecting the at least one first-level semiconductor device comprises forming or positioning intermediate conductive elements between bond pads of the at least one first-level semiconductor device and corresponding conductors of the interposer.

6. (Previously presented) The method of claim 1, wherein electrically connecting the second-level semiconductor device comprises forming or positioning intermediate conductive elements between bond pads of the second-level semiconductor device and corresponding conductors of the interposer.

7. (Previously presented) The method of claim 1, wherein positioning the second-level semiconductor device comprises at least one of positioning the second-level semiconductor device in a flip-chip arrangement over the at least one first-level semiconductor device and positioning the second-level semiconductor device over the interposer.

8. (Original) The method of claim 7, further comprising securing the at least one first-level semiconductor device and the second-level semiconductor device to one another before the positioning the second-level semiconductor device.

9. (Original) The method of claim 1, wherein the providing the interposer comprises providing a multi-interposer substrate on which the at least one first-level semiconductor device and the second-level semiconductor device are positioned and electrically connected.

10. (Original) The method of claim 9, further comprising singulating individual assemblies or packages from the multi-interposer substrate.

11. (Original) The method of claim 2, further comprising adhering a film to the lower surface of the substrate to cover at least a portion of the receptacle prior to positioning the at least one first-level semiconductor device therein.

12. (Previously presented) The method of claim 11, further comprising removing the adhered film from the lower surface following curing of the encapsulant material in the receptacle.

13. (Previously presented) The method of claim 1, further comprising positioning another first-level semiconductor device within the receptacle, a backside of the another first-level semiconductor device facing the backside of the at least one first-level semiconductor device.

14. (Previously presented) The method of claim 13, further comprising electrically connecting bond pads of the another first-level semiconductor device to corresponding conductors on the lower surface of the substrate.

15. (Previously presented) The method of claim 13, further comprising positioning a third-level semiconductor device over the lower surface of the substrate.

16. (Original) The method of claim 15, further comprising electrically connecting bond pads of the another first-level semiconductor device to corresponding bond pads of the third-level semiconductor device.

17. (Original) The method of claim 15, further comprising electrically connecting bond pads of the third-level semiconductor device to corresponding conductors on the lower surface of the substrate.

18. (Currently amended) A method for assembling semiconductor device components, comprising:

providing an interposer with a substantially planar, substantially rigid substrate and a receptacle formed substantially through the substrate;

positioning a first semiconductor device over a first surface of the interposer, at least one bond pad of the first semiconductor device being exposed to the receptacle;

positioning a second semiconductor device over a second surface of the interposer, at least one bond pad of the second semiconductor device being exposed to the receptacle; and

electrically connecting the at least one bond pad of the first and second semiconductor devices through the receptacle; and

electrically connecting at least the first semiconductor device to the interposer, at least a laterally extending portion of one conductive element carried by a surface of the first semiconductor ~~device~~ device, also facilitating electrical connection of the second semiconductor device to the interposer upon electrically connecting the at least the first semiconductor device thereto.

19. (Previously presented) The method of claim 18, wherein electrically connecting includes securing a conductive structure to the at least one bond pad of the first semiconductor device or to the at least one bond pad of the second semiconductor device.

20. (Original) The method of claim 19, wherein securing is effected before positioning.

21. (Original) The method of claim 19, wherein securing is effected following positioning.

22. (Original) The method of claim 18, wherein positioning the first semiconductor device comprises positioning the first semiconductor device with the at least one bond pad exposed to the receptacle comprising a portion of a redistribution circuit on a surface of the first semiconductor device.